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Appl. No. 10/015,887*Amendments to the Claims*

1. (Canceled)
2. (Previously Amended) A differential amplifier, comprising:
 - a differential input capable of receiving a differential signal;
 - a first differential pair coupled to said differential input;
 - a second differential pair, coupled to said differential input, and connected in parallel with said first differential pair at a differential output;
 - a differential offset circuit, coupled between said differential input and said second differential pair, and capable of level shifting said differential signal from a first level to a second level; and
 - a differential switch circuit, coupled to said first differential pair and said second differential pair, and capable of controlling a first current flow to said first differential pair and a second current flow to said second differential pair.
3. (Canceled)
4. (Canceled)
5. (Original) A differential amplifier, comprising:
 - a differential input capable of receiving a differential signal;
 - a first differential pair coupled to said differential input;

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a second differential pair, coupled to said differential input, and connected in parallel with said first differential pair at a differential output; and

a differential switch circuit, coupled to said first differential pair and said second differential pair, and capable of controlling a first current flow to said first differential pair and a second current flow to said second differential pair.

6. (Original) The differential amplifier of claim 5, further comprising:

a differential offset circuit, coupled between said differential input and said second differential pair, and capable of level shifting said differential input signal from a first level to a second level.

7. (Original) The differential amplifier of claim 5, wherein said differential switch circuit comprises:

a first switch MOSFET coupled between said first differential pair and a current source; and

a second switch MOSFET coupled between said second differential pair and said current source.

8. (Original) A differential amplifier, comprising:

a differential input capable of receiving a differential input signal;

a first differential pair coupled to said first differential input, said first differential pair biased with a first power supply voltage and a second power supply voltage;

a second differential pair, coupled to said differential input, and connected in parallel with said first differential pair at a differential output, said second differential

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pair biased with said first power supply voltage and said second power supply voltage;
and

a differential switch circuit, coupled to said first differential pair and said second differential pair, and capable of controlling a first current flow to said first differential pair and a second current flow to said second differential pair.

9. (Original) The differential amplifier of claim 8, wherein said differential switch circuit changes said first current flow relative to said second current flow, based on a comparison between a common mode voltage of said differential input signal and a reference voltage.

10. (Original) The differential amplifier of claim 8, wherein said differential switch circuit increases said first current flow relative to said second current flow, when a common mode voltage of said differential input signal approaches said first power supply voltage.

11. (Original) The differential amplifier of claim 8, wherein said differential switch circuit decreases said first current flow relative to said second current flow, when a common mode voltage of said differential input signal approaches said second power supply voltage.

12. (Canceled)

13. (Canceled)

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14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Currently Amended) A method of extending an input signal range of a component that receives the input signal, comprising the step of:

- (1) level shifting a voltage of the input signal;
- (2) processing said level shifted voltage within the component; and
- (3) selecting a subcomponent, from a plurality of subcomponents within the component, to process said ~~offset~~ level shifted voltage.

20. (Currently Amended) ~~The A method of claim 19, wherein step (3) comprises~~
extending an input signal range of a component that receives the input signal, comprising
the ~~step~~ steps of:

- (1) level shifting a voltage of the input signal;
- (2) processing said level shifted voltage within the component; and

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(3) responding to a comparison between a common mode voltage of the input signal and a reference voltage to select ~~said a~~ subcomponent from ~~said a~~ plurality of subcomponents within the component to process said ~~offset~~ level shifted voltage.

21. (Previously Presented) The method of claim 19, wherein step (2) comprises the step of:

amplifying said level shifted voltage within the component.